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Design Example: Binary Counter • Synchronous 4-bit binary counter • Incremented by a count of 1 at each active edge of the clock • Wrap count to 0 when the count reaches 1111 2. Implicit machine: register transfer operation ($\text{count} \leq \text{count} + 1$) conditionally, in every clock cycle, depending on enable

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Advanced Digital Design with the Verilog HDL

His areas of interest include Modeling, synthesis and verification of digital systems with hardware description languages, system-level design languages, and embedded systems with FPGAs. He is the author of Advanced Digital Design with the Verilog HDL and the co-author of Digital Design, 4e.

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It is an advanced digital logic design textbook that emphasizes the use of synthesizable Verilog code and provides numerous fully worked-out practical design examples including a Universal Serial Bus interface, a pipelined multiply-accumulate unit, and a pipelined microprocessor for the ARM THUMB architecture.

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