

Arm Primecell Technical Reference Manual

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~~• Arm® CoreLink™ SIE-200 System IP for Embedded Technical Reference Manual (Arm DDI 0571). • Arm® Cortex®-M System Design Kit Technical Reference Manual (Arm DDI 0479). • Arm® Cortex®-M33 Processor Technical Reference Manual (Arm 100230). • PrimeCell® UART (PL011) Technical Reference Manual (Arm DDI 0183).~~

~~ARM PrimeCell Synchronous Serial Port (PL022) Technical ...~~

The reset controller generates the power-on reset, nPOR, and AMBA reset signal, HRESETn. The MPMCBIGENDIAN, MPMCSTCS1MW[1:0], and MPMCSTCS[3:0]POL signals are generated by registering the value of several inputs to the chip when the power-on reset goes inactive. These input signals are reused during normal operation.

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This is the ARM Technical Reference Manual (TRM) for the ARM PrimeCell® UART (PL010). It contains a functional description of the product and is primarily aimed at design engineers.

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~~PrimeCell AHB SDR and SRAM/NOR Memory ...—ARM architecture~~

~~• Arm® PrimeCell Real Time Clock (PL031) Technical Reference Manual (DDI 0224). • CoreSight™ Components Technical Reference Manual (DDI 0314). • Arm® DS-5 Arm DSTREAM User Guide (DUI 0481).~~

~~PrimeCell® DMA Controller (PL330) Technical Reference Manual~~

Figure 2.16 shows the timing diagram for a single external memory write transfer with minimum zero wait states where the SMC does not have control of the bus and must request for it using an external synchronous bus multiplexor when a device such as an SDRAM controller is used. In this example nothing else is requesting the bus, so the SMC is granted straight away, showing the minimum timing ...

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Undefined length INCR bursts

~~ARM PrimeCell General Purpose Input/Output (PL061 ...~~

The PrimeCell Synchronous Serial Port (SSP) is an Advanced Microcontroller Bus Architecture (AMBA) slave block that connects to the Advanced Peripheral Bus (APB). The PrimeCell SSP is an AMBA compliant System-on-Chip (SoC) peripheral that is developed, tested, and licensed by ARM. The PrimeCell SSP is a master or slave interface that enables synchronous serial communication with slave or ...

~~ARM PrimeCell MultiPort Memory Controller (PL176 ...~~

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ARM PrimeCell General Purpose Input/Output (PL061) Technical Reference Manual . Preface; Introduction; Functional Overview. PrimeCell GPIO overview; PrimeCell GPIO functional description. AMBA APB interface; Interrupt detection logic; Mode control; PrimeCell GPIO operation; Programmer's Model; Programmer's Model for Test; Signal Descriptions

~~ARM PrimeCell Real Time Clock (PL031) Technical Reference ...~~

This is the ARM Technical Reference Manual (TRM) for the PrimeCell® DMA Controller (PL330) Revision:r0p0. It contains a functional description of the product and is primarily aimed at design engineers.

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