Cadence Encounter User Manual

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Frogkicknl, Pablo Oubre Cadence Design Systems - Cadence Encounter Timing System User Manual. Encounter RTL Compiler allows engineers to look across the entire design as System placement technology into synthesis, providing real physical timing. Primary tools from Cadence Design Systems, Inc., form the mainstay of The static timing

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Yogesh Bansal and Aditi Bagree, from the Cadence TFO team, through their application note, "Physical Synthesis using RTL Compiler Achieving Best Quality-of-Silicon", talk about using "physical synthesis" aspects for design closure. The document is based on the 12.1 release of RTL Compiler, and captures the basic flow that needs to be followed.

~~Innovus Implementation System - cadence.com~~
Page 1 EnCounTEr DIAgnoSTICS Yield loss is one of the biggest challenges with sub-90nm designs. Traditional in-line inspection techniques cannot keep with pace with the increasing number of subtle design-process variations. Cadence Encounter Diagnostics is the industry's ® ® first yield diagnostics technology proven to accelerate yield ramp in manufacturing environments.

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Are you designing a 5G or radar application, or for that matter any application, that requires RF components? Are cost, size-reduction, and performance improvement major concerns for you? Most probably they are. Here we talk about an innovative solution for mixed-signal RF designs using Cadence layout editors.

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Page 1 ENC OU N TE R D IG ITA L IMPL EME N TAT ION S Y ST E M Cadence Encounter Digital Implementation System refines ® ® and redefines digital implementation, helping customers deliver differentiated products to their end market, achieve predictable time to market with the highest quality silicon, and reduce development and production costs.; Page 2 • Scalability in performance - Delivers ...

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The Tempus Timing Signoff Solution has been our timing tool for all of our SoCs that enable smart TV, set-top boxes and media connectivity. Its runtime performance, coupled with integration within the Cadence Innovus™ Implementation System, has allowed us to significantly reduce the time we spend in timing signoff.

~~Tempus Timing Signoff Solution - Cadence~~
Cadence is a leading EDA and Intelligent System Design provider delivering tools, software, and IP to help you build great products that connect the world

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Cadence® Encounter® Digital Implementation (EDI) System provides the most effective methodology to maximize performance, and minimize power and area for high-performance, 100M+ instance, and power-efficient designs. Integration with the Cadence Virtuoso® custom design environment ensures

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Cadence Genus Synthesis Solution is a next-generation RTL synthesis and physical synthesis tool that delivers up to 10X better RTL design productivity with up to 5X faster turnaround times.

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The Cadence Innovus Implementation System is a physical implementation tool that delivers typically 10-20% production-proved power, performance, and area (PPA) advantages along with up to 10X turnaround time (TAT) gain in advanced 16/14/7/5nm FinFET designs as well as at established process nodes.

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Page 1 ENCOUNTER CONFORMAL CONSTRAINT DESIGNER Cadence Encounter Conformal Constraint Designer, a key ® ® ® component of the Cadence Logic Design Team Solution, automates the validation, generation, and refinement of SDC timing constraints. By ensuring that timing constraints are valid throughout the entire design process, and by pinpointing real design issues early, quickly, and accurately ...

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Page 1 ENCOU N TE R C O N FOR MA L EQUIVA LE N C E C H EC K ER Cadence Encounter Conformal Equivalence Checker (EC), ® ® ® makes it possible to verify and debug multi-million-gate designs without using test vectors. It offers the only complete equivalence checking solution available for verifying SoC designs—from RTL to final LVS netlist (SPICE)—as well as FPGA designs.